REMARKS

The Office Action of July 12, 2004 has been carefully considered. In response thereto, the claims have been amended as set forth above. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claim 1 has been amended to clarify the location of the scan chain partitions on the boundary of the electronic device: " ...a first shift register having a plurality of cells and a second shift register having a plurality of cells, each cell of the first shift register being coupled between an external pin and one of the test arrangements from the first plurality of test arrangements and each cell of the second shift register being coupled between an external pin and one of the test arrangements from the second plurality of test arrangements...". This amendment is allowed because it finds its basis in the application as originally filed; see for instance page 9 line 5-7 of the originally filed application.

It is emphasized that reference WHETSEL in the communication does not disclose a plurality of scan chains on the boundary of an electronic device; WHETSEL is directed to testing so-called systems on chip (SoCs), in which an IC has multiple independent functional blocks (cores 110, 120) that need to be independently testable in an efficient way. To this end, each core is extended with a test control block (122, 132), with the test control blocks being interconnected via a serial data path. This serial data path is internal to the IC, and not every cell of the serial path is connected to an external pin, in contrast to the present invention.

The present invention is directed to testing ICs that have a plurality of internal scan chains, which may be an arrangement as disclosed in WHETSEL. However, whereas each internal scan chain in WHETSEL is directly connected to an external pin (WHETSEL, col. 2 line 45-47), the internal scan chains of the present invention receive their data through a boundary scan chain, which may be compliant with the IEEE 1149.1 standard. It is known

to use a single boundary scan chain for such a purpose in order to reduce the number of pins that need connecting to an test apparatus to provide the device under test with the appropriate test patterns. In fact, the IEEE 1149.1 standard dictates the presence of a single test data in (TDI) and a single test data out (TDO) pin. Thus, there is a technical prejudice against using more than one pin to feed test (result) data into or out of a partitioned boundary scan chain or a plurality of smaller boundary scan chains, which renders the present invention non-obvious over known use of a boundary scan chain to communicate with the internals of an IC during test. In particular, combination of WHETSEL with these teachings would lead to an arrangement in which the internal scan chains of WHETSEL are fed through a single pin of a boundary scan chain, in contrast to the feeding mechanism of the present invention, rendering the present invention inventive over WHETSEL in isolation as well as over WHETSEL in combination with the teachings of IEEE 1149.1. Moreover, it is emphasized that for the partitioning of a single scan chain into several sections a technical problem has to be overcome; to this end, the control protocols used for such a scan chain must be altered as explained on p. 11 line 12-29 of the originally filed application, which is again a clear indication of the presence of an inventive step.

The same argument applies *mutatis mutandis* to the claims 20 and 21 directed to the testable electronic device.

Allowance of claims 16-21 is respectfully requested.

Respectfully submitted,

Michael J. Ure, Reg. 33,089

Dated: October 4, 2005